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EXAMINER
JOHNSON, BRIAN P

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

		Application No.	Applicant(s)
Office Action Summary		10/702,363	SINGH ET AL.
		Examiner	Art Unit	
		BRIAN P. JOHNSON	2183	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS,
WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>17 December 2007</u>.

2a)☒ This action is **FINAL.**   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>2,5-8,11-14,18,19,22-25 and 27-35</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>2, 5-8, 11-14, 18-19, 22-25, and 27-35</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
      application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 2, 5-8, 11-14, 18-19, 22-25, and 27-35 are pending.

Papers Filed

2.   Examiner acknowledges receipt of amendments and remarks filed on 17

December 2007.

Claim Rejections - 35 USC § 112

1.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter which the applicant regards as his invention.

2.   Claims 31-35 are rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention.

In particular, (a) and (b) mention "loop control parameters" while (d) mentions

"the loop control parameters." It is unclear which loop control parameters are being

referred to by (d). Furthermore, it is unclear whether (d) refers to either or both of the

speculative and architectural loop control parameters of (a).

Claim 34 contains a similar issue.

Claim Rejections - 35 USC § 102

3.   The following is a quotation of the appropriate paragraphs of 35

U.S.C. 102 that form the basis for the rejections under this section made in this Office

action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4.   Claims 2, 5-8, 11-14, 18-19, 22-25, and 27-35 are rejected under 35

U.S.C. 102(b) as being anticipated by Parthasarathy (U.S. Patent No. 6,671,799).

5.   As per claim 31, Parthasarathy discloses a method for issuing instructions in a

processor having a pipeline, comprising:

(a) providing a loop buffer (Fig. 2 loop buffer 212) for holding program loop

instructions and a register file (Fig. 2 loop setup 222) having at least three entries (Fig. 3

registers LER and LSR 0-2) for holding speculative and architectural loop control

parameters (Col. 6 lines 65-67) *The examiner asserts that any parameters stored in*

register file 222 which are not part of an active loop are speculative, and those which

are a part of an active loop are architectural

wherein each entry in the register file comprises a loop top register for holding a loop

top address, a loop bottom register for holding a loop bottom address and a loop

count register for holding a loop count (Col. 1 lines 34-36 and Col. 7 lines 49-57).

(b) in response to decoding of a first loop setup instruction, marking a first entry in the register file as a current entry and writing in the first entry loop control parameters represented in the first loop setup instruction; (Col. 7 lines 49-57) *The examiner asserts that while loop conditions are written to a set of registers, those registers must be selected before being written to and constitute current register entries.*

(c) sending the first loop setup instruction down the pipeline (col 7 lines 49-57);

(d) issuing loop instructions corresponding to the first loop setup instruction speculatively after the loop control parameters are written in the current entry in the register file and before the first loop setup instruction has completed execution in the pipeline, wherein the current entry in the register file contains speculative copies of the loop control parameters (col 6 lines 40-53); *Examiner asserts that the loop instruction is speculative because a system flush may be required* and

(e) marking the current entry in the register file as an architectural entry in response to the first loop setup instruction being committed in the pipeline; (Col. 7 lines 49-57 and col. 5 lines 31-33) *The examiner asserts that when a loop begins and the first instruction is matched to the loop start register (LSR0, 1 or 2),the setup is committed, the loop is begun and the selected loop start register and it's associated loop stop and loop count (LER and LCR) registers are considered to be architectural registers.*

6.   As per claim 32, Parthasarathy discloses the method of claim 31, including (f) sending a loop bottom indicator down the pipeline with a loop bottom instruction; and

The examiner asserts that Parthasarathy's invention inherently sends a loop bottom

indicator down the pipeline since one of registers LCR0, LCR1 and LCR2 contains the

active loop count. If no loop bottom indicator arrived at the architectural registers, the

count would never decrement and the loop would never exit, causing undesired

operation.

1.   As per claim 33, Parthasarathy discloses the method of claim 32, including (g)

selecting, the loop top address of the current entry from the loop top addresses in the

register file, comparing, in a single loop top comparator, a current instruction address

with the selected loop top address to determine a loop top match, selecting the loop

bottom address of the current entry from the loop bottom addresses in the register file,

and comparing, in a single loop bottom comparator, the current instruction address with

the selected loop bottom address to determine a loop bottom match (col 2 lines 8-30).

1.   As per claim 34, this claim is rejected under the same grounds as claim 31.

2.   As per claim 33, this claim is rejected under the same grounds as claim 35.

6.   As per claim 2, Parthasarathy discloses a method as defined in claim 31, further

comprising decrementing a loop count in the architectural entry in the register file in

response to the loop bottom instruction being committed in the pipeline. (Col. 8 lines 57-

60)

7.   As per claim 5, Parthasarathy discloses a method as defined in claim 31, further

comprising generating a current pointer to the current entry in the register file and

generating an architectural pointer to the architectural entry in the register file.   *The*

examiner asserts that any time a set of loop registers is updated, information must be

decoded to label it as a current register. The current registers are labeled as such by

the incoming Loop Setup signals in Fig. 3 (Col. 7 lines 49-57). The architectural entry is

determined to be so by matching the PC with the addresses stored in the loop registers.

(Col. 5 lines 31-33)

8.   As per claim 6, Parthasarathy discloses a method as defined in claim 5, further

comprising incrementing the current pointer to a second entry in the register file in

response to decoding of a second loop setup instruction and writing in the second entry

loop control parameters represented in the second loop setup instruction. *The*

examiner asserts that a second entry is inherently selected by any second loop set up

instruction (Col. 7 lines 49-57). Once a loop register is selected, it becomes current as

it is being written.

9.   As per claim 7, Parthasarathy discloses a method as defined in claim 6, further

comprising incrementing the architectural pointer to the second entry in the register file

in response to the second loop setup instruction being committed. *The examiner*

asserts that when a loop begins and the first instruction is matched to the loop start

register (LSR0, 1 or 2), the setup is committed, the loop is begun and the selected loop

start register and it's associated loop stop and loop count (LER and LCR) registers are

considered to be architectural registers.

10.   As per claim 8, Parthasarathy discloses a method as defined in claim 6, further

comprising moving the current pointer to a location of the architectural pointer in

response to an interrupt or a pipeline abort. (Col. 6 lines 54-66) *The examiner asserts*

that a loop flush constitutes an interrupt of processing. When such a flush happens, the

loop setup registers are consulted, making them current registers.

11.   As per claim 11, Parthasarathy discloses a method as defined in claim 31, further

comprising writing a temporary loop count in a temporary loop count register and

decrementing the temporary loop count on each loop bottom match. *The examiner*

asserts that the LCR is a temporary loop count register. The value held therein remains

at a value for a limited amount of time before being decremented to a new value. (Col. 8

lines 57-60)

12.   As per claim 12, Parthasarathy discloses a method as defined in claim 11, further

comprising exiting the program loop when the temporary loop count has decremented to

zero. (Col. 5 lines 46-60)

13.   As per claim 13, Parthasarathy discloses a method as defined in claim 31, further comprising stalling a loop setup instruction when the register file does not have an available entry. *The examiner asserts that a loop setup instruction must inherently be stalled if no destination registers are available. If the setup instruction was not stalled, the processor may break from the current loop before the count register reached zero, causing undesired operation.*

14.   As per claim 14, Parthasarathy discloses a method as defined in claim 31, wherein instructions are issued without sending the loop control parameters down the pipeline. *The examiner asserts that the loop control parameters reside in the loop control registers (LSR, LER, LCR) and do not travel down the pipeline with issued instructions.*

15.   As per claim 18, Parthasarathy discloses an apparatus as defined in claim 34, wherein the controller further comprises means for, sending a loop bottom indicator down the pipeline with a loop bottom instruction, and decrementing a loop count in the architectural entry in the register file in response to the loop bottom instruction has completed execution in the pipeline. (Col. 8 lines 57-60) *The examiner asserts that Parthasarathy's invention inherently sends a loop bottom indicator down the pipeline since one of registers LCR0, LCR1 and LCR2 contains the active loop count. If no loop bottom indicator arrived at the architectural registers, the count would never decrement and the loop would never exit, causing undesired operation.*

16.   As per claim 19, Parthasarathy discloses an apparatus as defined in claim 18,

wherein the controller further comprises means for marking a second entry in the

register file as the current entry in response to decoding of a second loop setup

instruction and for writing in the second entry loop control parameters represented in the

second loop setup instruction, and means for marking the second entry in the register

file as the architectural entry in response to the second loop setup instruction has

completed execution in the pipeline. *The examiner asserts that a second entry is*

inherently selected by any second loop set up instruction (Col. 7 lines 49-57). Once a

loop register is selected, it becomes current as it is being written. The examiner asserts

that when a loop begins and the first instruction is matched to the loop start register

(LSR0, 1 or 2), the setup is committed, the loop is begun and the selected loop start

register and it's associated loop stop and loop count (LER and LCR) registers are

considered to be architectural registers.

1.   As per claim 22, Parthasarathy discloses an apparatus performing the method of

claim 34. Therefore, calim 22 is rejected under the same grounds as claim 11 listed

above.

17.   As per claim 23, Parthasarathy discloses an apparatus performing the method of

claim 12. Therefore, claim 23 is rejected under the same grounds as claim 12 listed

above.

18.   As per claim 24, Parthasarathy discloses an apparatus performing the method of claim 13. Therefore, claim 24 is rejected under the same grounds as claim 13 listed above.

19.   As per claim 25, Parthasarathy discloses an apparatus performing the method of claim 34. Therefore, claim 25 is rejected under the same grounds as claim 14 listed above.

20.   As per claim 27, Parthasarathy discloses an apparatus performing the method of claim 5. Therefore, claim 27 is rejected under the same grounds as claim 5 listed above.

21.   As per claim 28, Parthasarathy discloses an apparatus performing the method of claim 6. Therefore, claim 28 is rejected under the same grounds as claim 6 listed above.

22.   As per claim 29, Parthasarathy discloses an apparatus performing the method of claim 7. Therefore, claim 29 is rejected under the same grounds as claim 7 listed above.

23.   As per claim 30, Parthasarathy discloses an apparatus performing the method of

claim 8. Therefore, claim 30 is rejected under the same grounds as claim 8 listed

above.

Response to Arguments

1.   Applicant's arguments filed 17 December 2007 have been fully considered but

they are not persuasive. See rejection of claim 31.

Conclusion

The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

Inoue et al. (U.S. Publication No. 2002/0078333) disclose a hardware loop system

comprising "early" registers in addition to architectural registers for storing loop control

parameters.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

2.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

        If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

        Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183